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Jang et al.

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(54) **WAFER LEVEL LIGHT-EMITTING DIODE ARRAY AND METHOD FOR MANUFACTURING SAME**

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Jul. 26, 2013 (KR) 10-2013-0088710

(51) **Int. Cl.**
H01L 27/15 (2006.01)
H01L 33/38 (2010.01)
(Continued)

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CPC ..... ***H01L 27/156*** (2013.01); ***H01L 33/42*** (2013.01); *H01L 33/382* (2013.01); *H01L 33/385* (2013.01);*H01L 33/405* (2013.01); *H01L 33/44* (2013.01); *H01L 33/46* (2013.01); *H01L 33/62* (2013.01); *H01L 2933/0016* (2013.01); *H01L 2933/0025* (2013.01)

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USPC 438/29; 257/E21.211, E21.158, 257/E33.061
See application file for complete search history.

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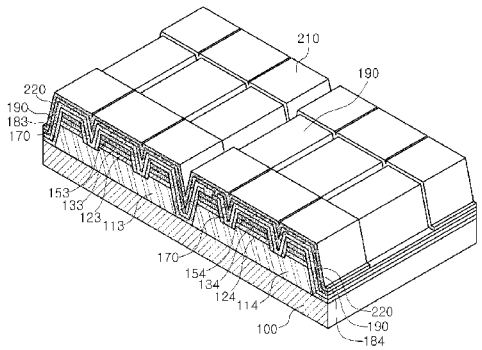
Primary Examiner — Evan Pert
Assistant Examiner — Changhyun Yi
(74) *Attorney, Agent, or Firm* — Perkins Coie LLP

(57) **ABSTRACT**

Disclosed are a light emitting diode array on a wafer level and a method of forming the same. The light emitting diode array includes a growth substrate; a plurality of light emitting diodes arranged on the substrate, wherein each of the plurality of light emitting diodes has a first semiconductor layer, an active layer and a second semiconductor layer; and a plurality of upper electrodes arranged on the plurality of light emitting diodes and formed of an identical material, wherein each of the plurality of upper electrodes is electrically connected to the first semiconductor layer of a respective one of the light emitting diodes. At least one of the upper electrodes is electrically connected to the second semiconductor layer of an adjacent one of the light emitting diodes, and another of the upper electrodes is insulated from the second semiconductor layer of an adjacent one of the light emitting diodes. Accordingly, it is possible to provide a light emitting diode array that can be driven under at a high voltage and simplify a forming process thereof.

26 Claims, 11 Drawing Sheets



(51) **Int. Cl.**

H01L 33/42	(2010.01)
H01L 33/44	(2010.01)
H01L 33/40	(2010.01)
H01L 33/46	(2010.01)
H01L 33/62	(2010.01)

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Fig. 1

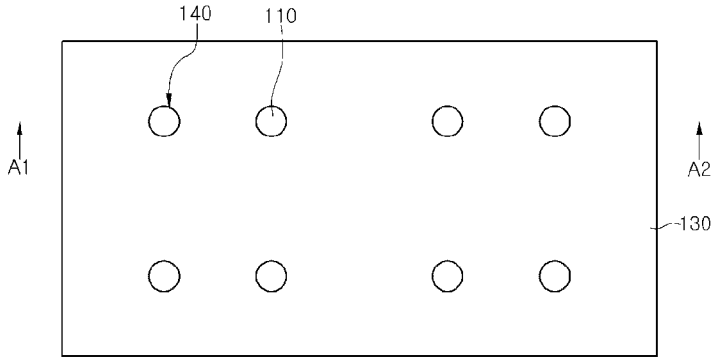
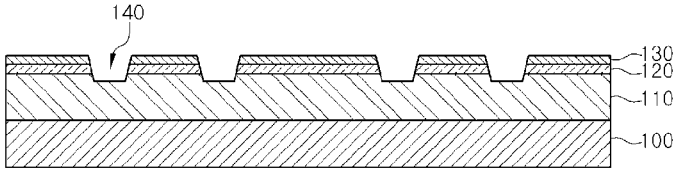


Fig. 2



A1 – A2

Fig. 3

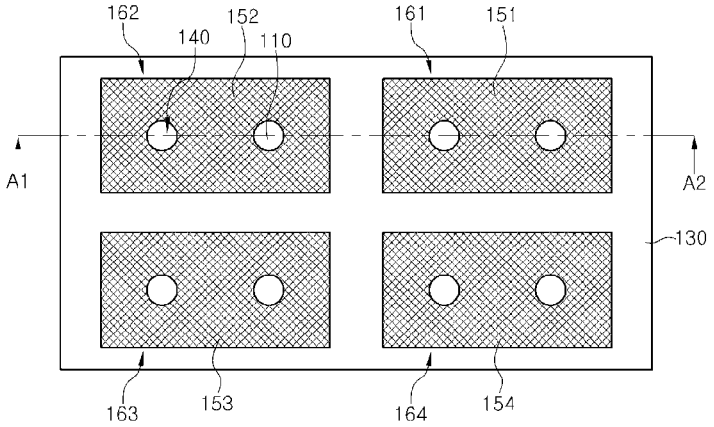
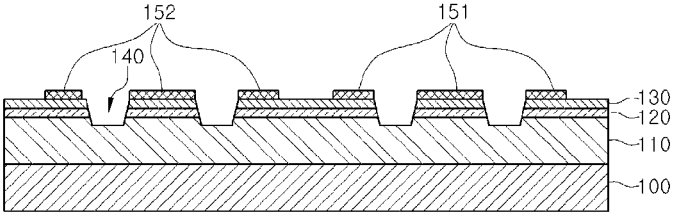


Fig. 4



A1 – A2

Fig. 5

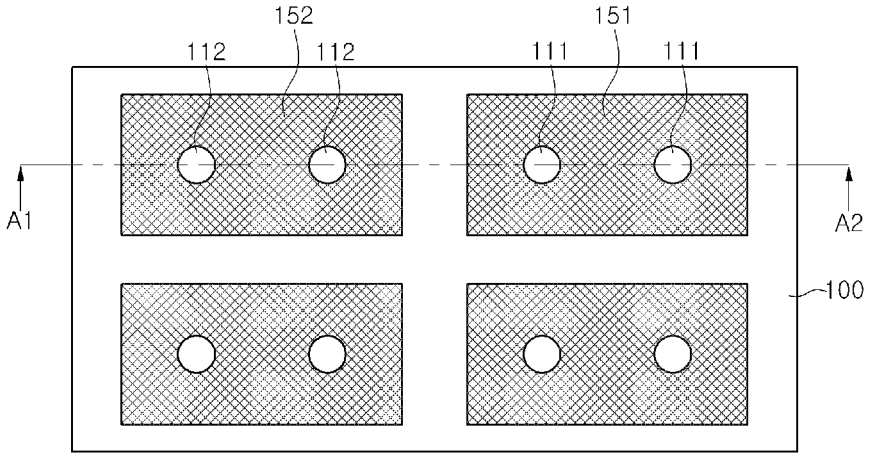
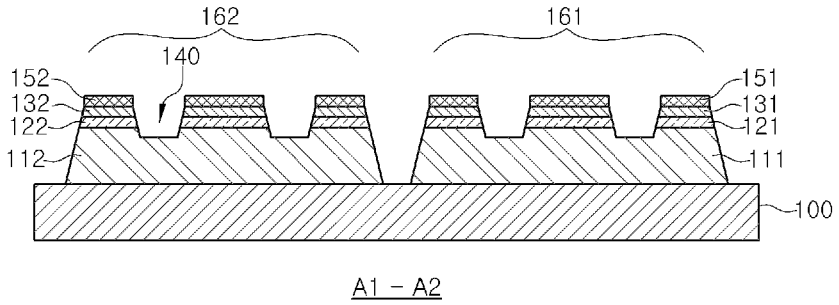


Fig. 6



A1 – A2

Fig. 7

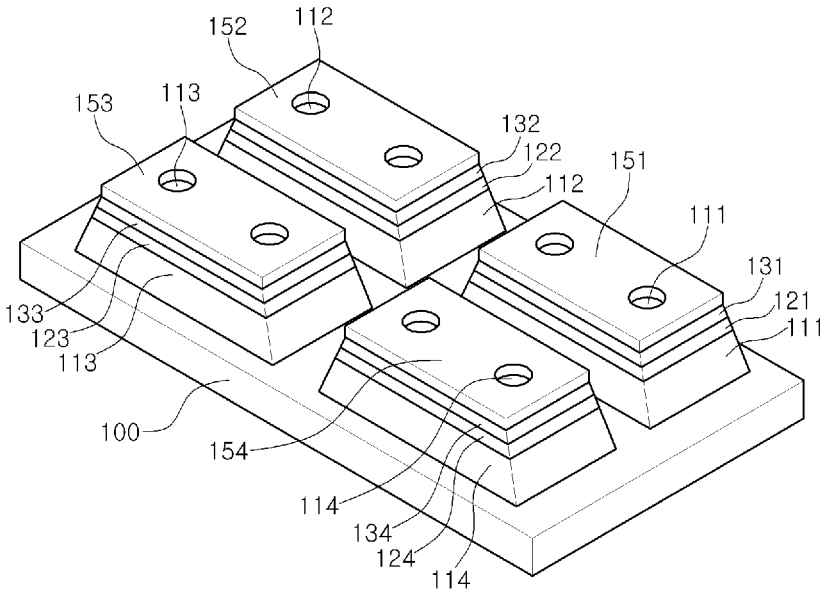
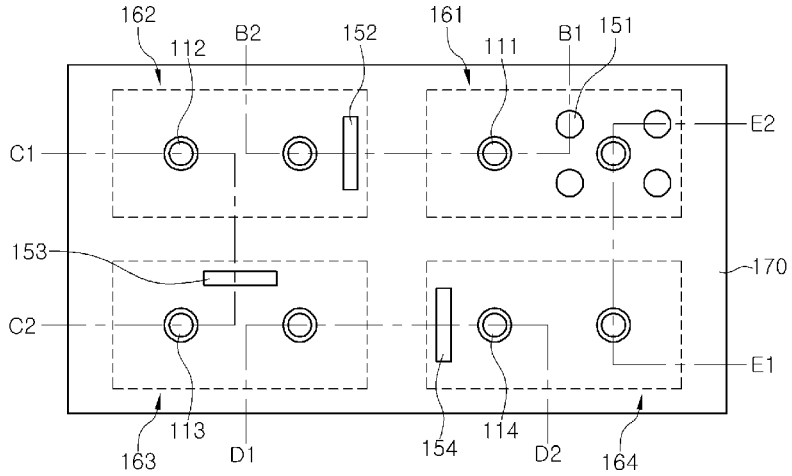


Fig. 8



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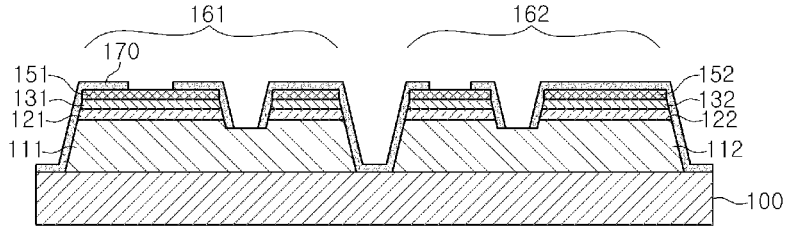
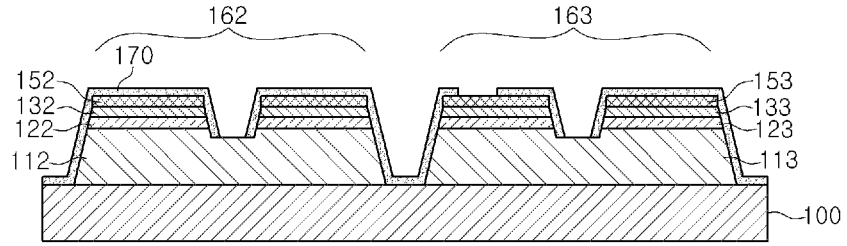


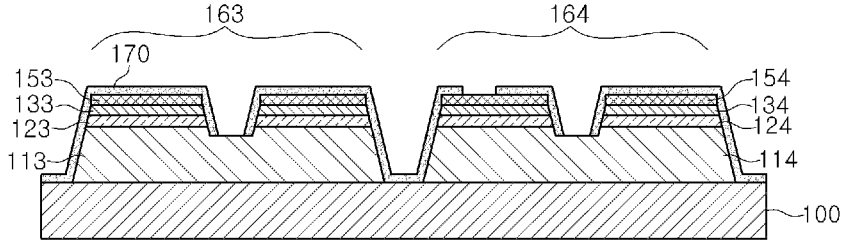
B1 – B2

Fig. 10



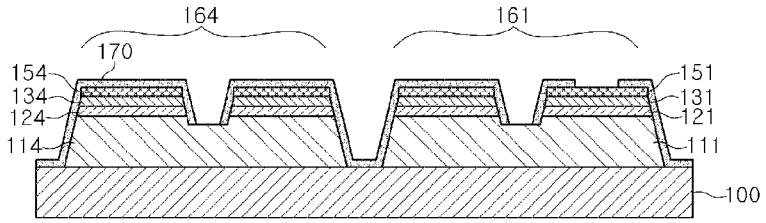
C1 – C2

Fig. 11



D1 – D2

Fig. 12



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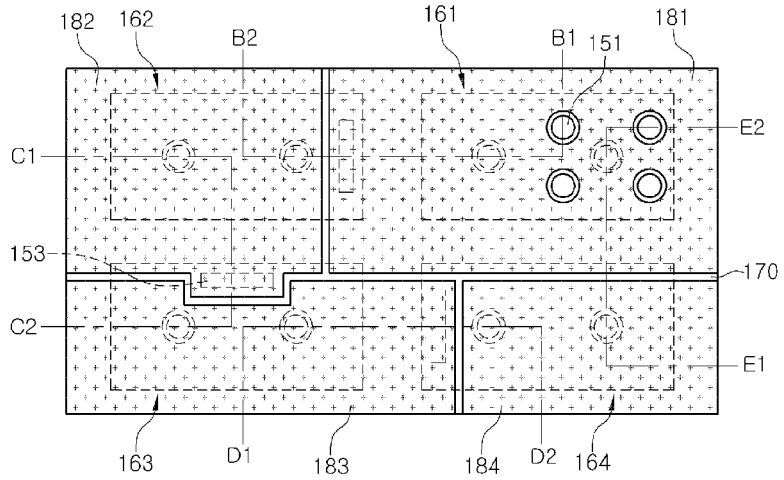

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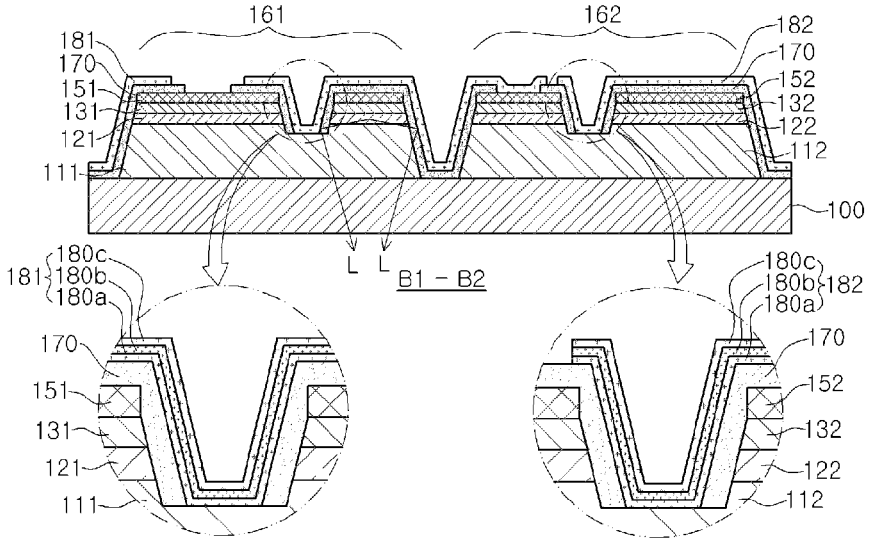
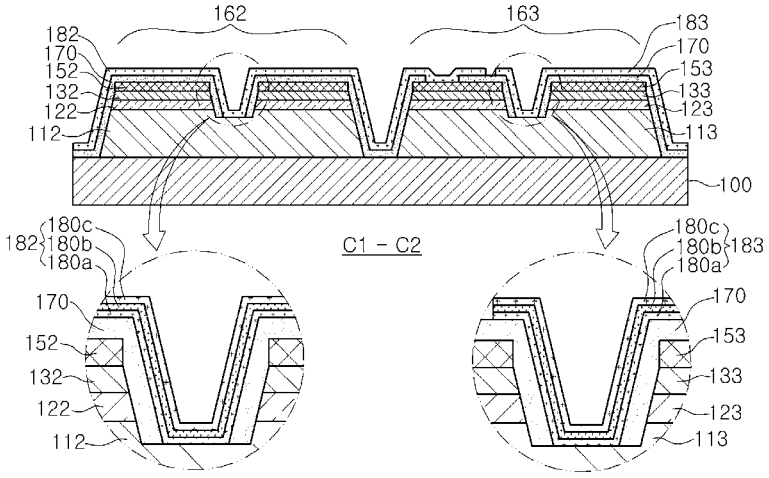


Fig. 15



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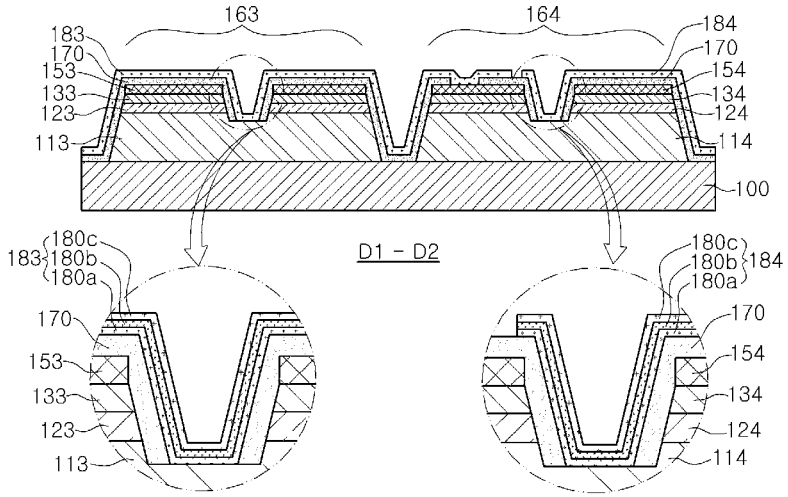

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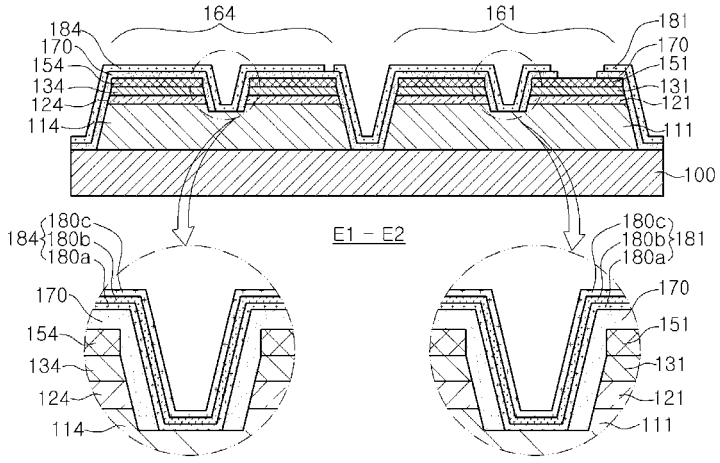

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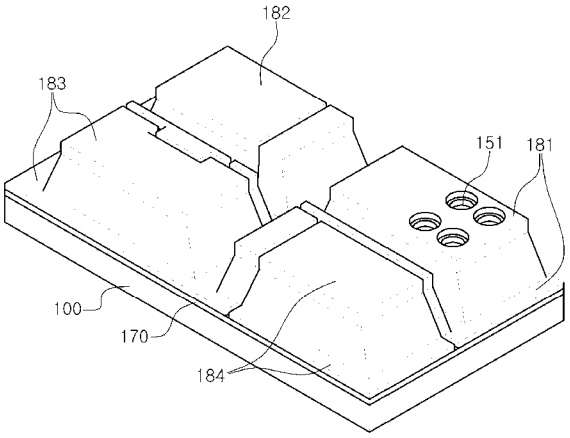


Fig. 19

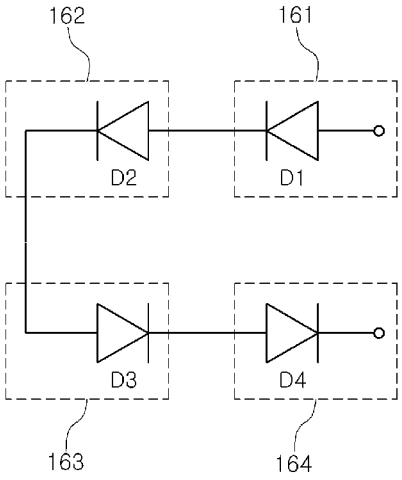


Fig. 20

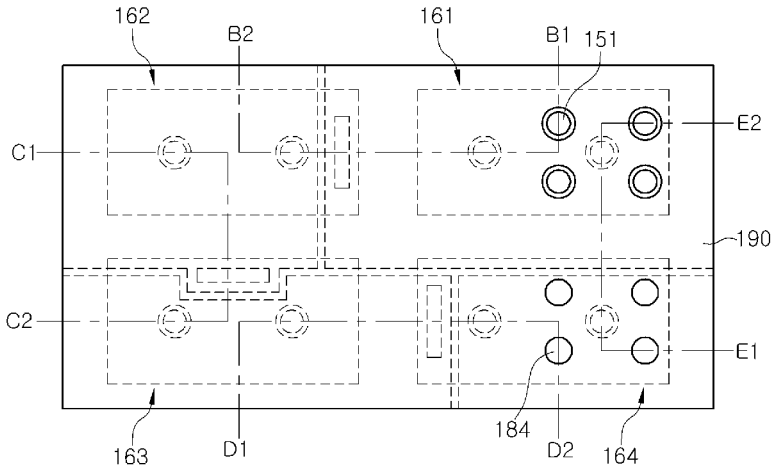
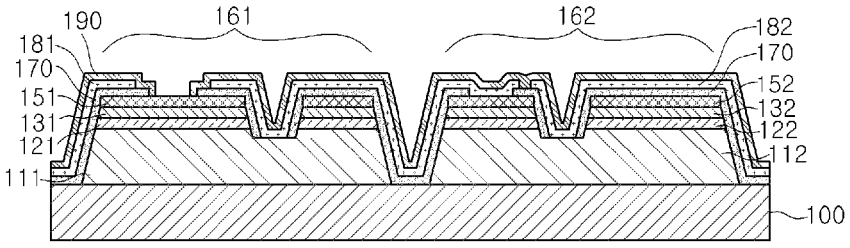
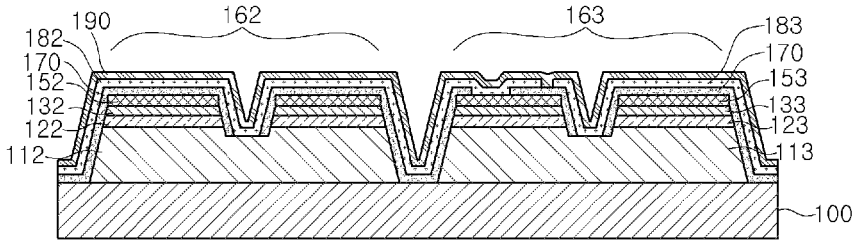


Fig. 21



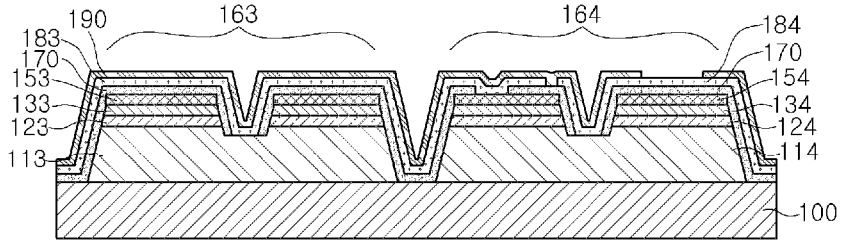
B1 - B2

Fig. 22



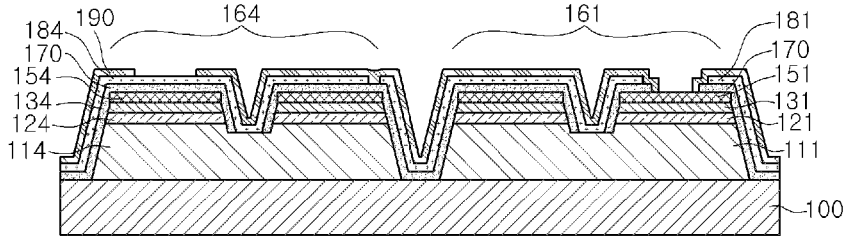
C1 - C2

Fig. 23



D1 - D2

Fig. 24



E1 - E2

Fig. 25

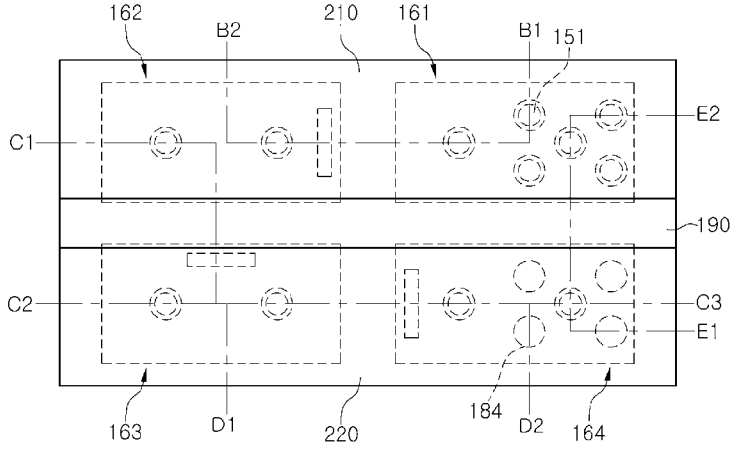
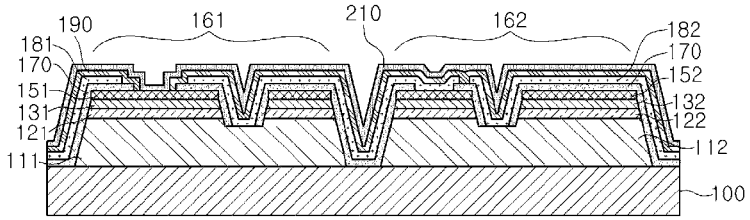
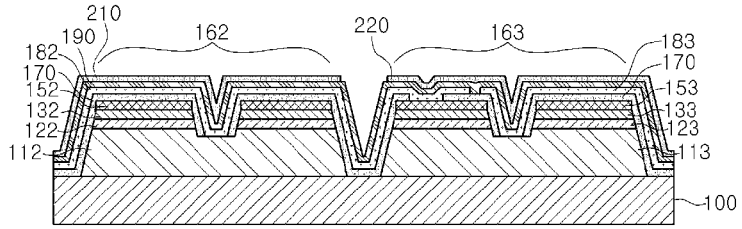


Fig. 26



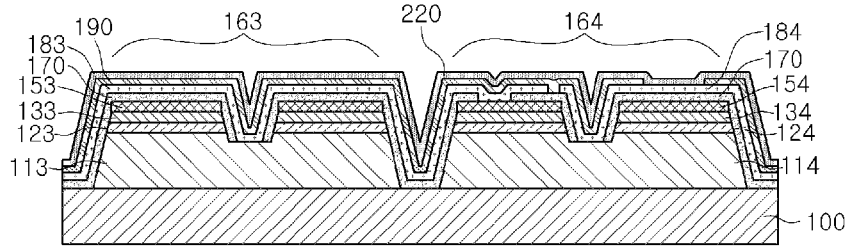
B1 - B2

Fig. 27



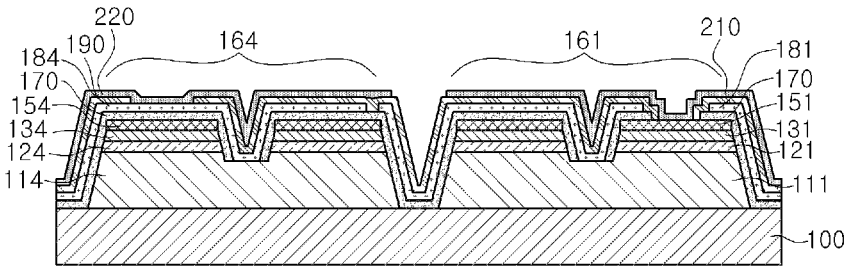
C1 - C2

Fig. 28



D1 - D2

Fig. 29



E1 – E2

Fig. 30

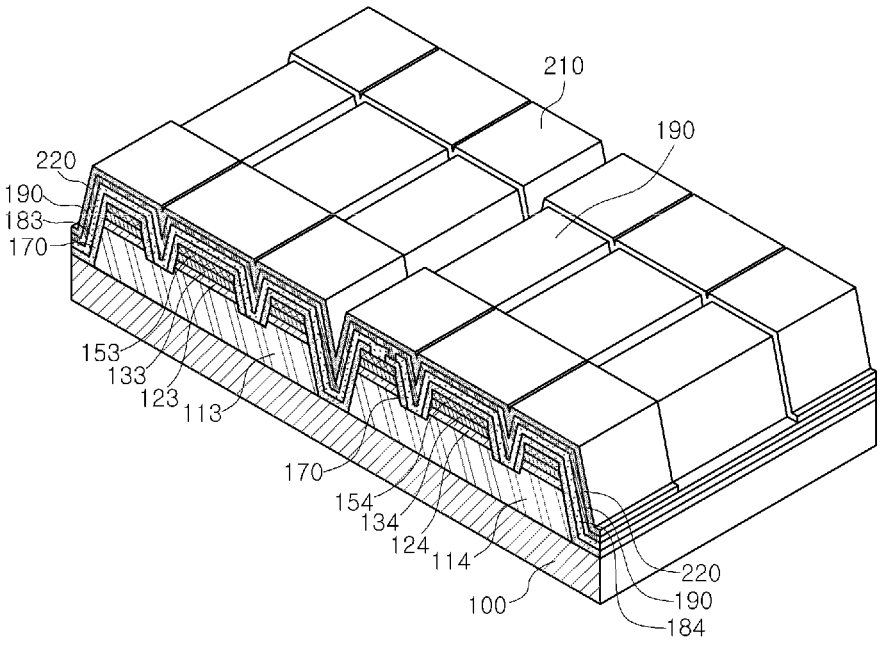


Fig. 31

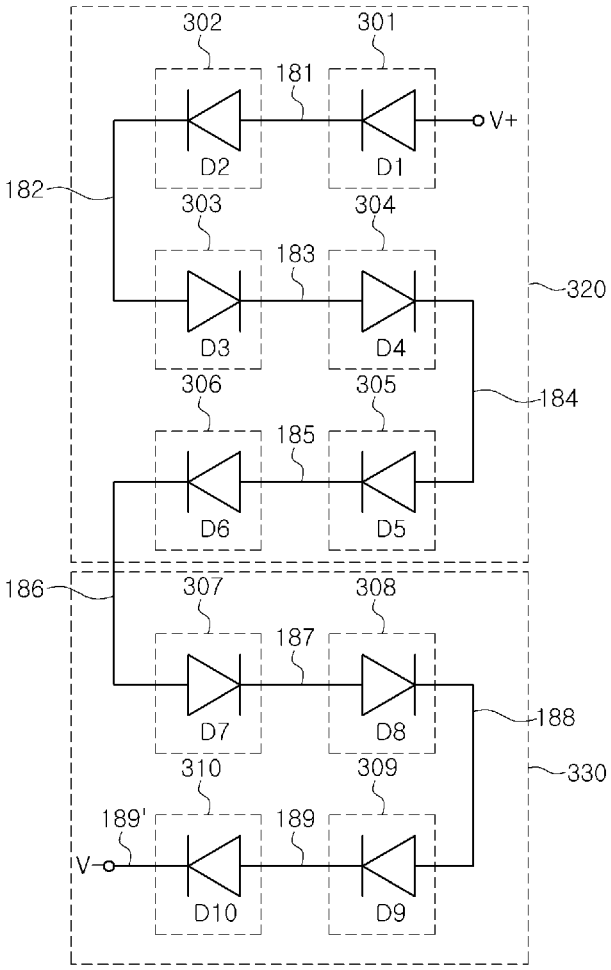

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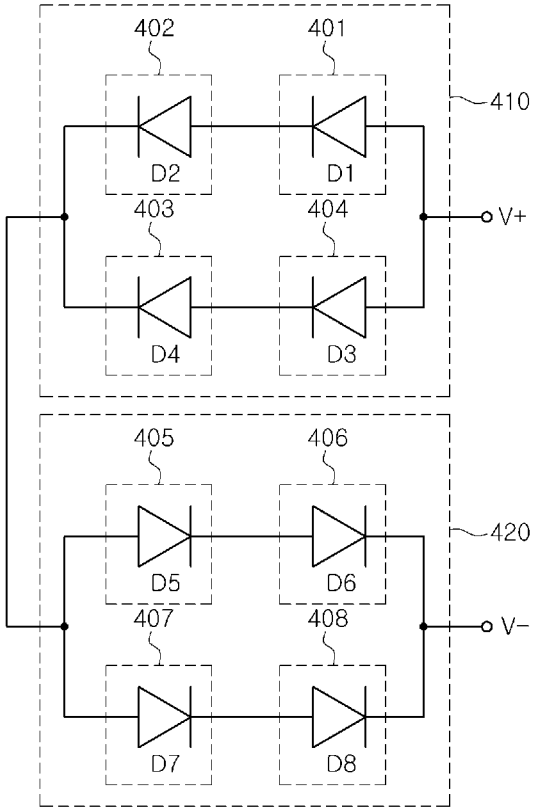
Fig. 32



WAFER LEVEL LIGHT-EMITTING DIODE ARRAY AND METHOD FOR MANUFACTURING SAME

CROSS REFERENCE TO RELATED APPLICATION

This patent document is a 35 U.S.C. 371 National Stage application of PCT Application No. PCT/KR2013/007091, filed on Aug. 6, 2013, which further claims the benefits and priorities of prior Korean Patent Application No. 10-2012-0086329, filed on Aug. 7, 2012, prior Korean Patent Application No. 10-2012-0094107, filed on Aug. 28, 2012, prior Korean Patent Application No. 10-2013-0088709, filed on Jul. 26, 2013, and prior Korean Patent Application No. 10-2013-0088710, filed on Jul. 26, 2013. The entire disclosures of the above applications are incorporated by reference as part of this document.

TECHNICAL FIELD

The present invention relates to a light emitting diode array, and more particularly, to a light emitting diode array with a plurality of light emitting diodes connected through wires and formed into a flip chip type, and a method of forming the same

BACKGROUND ART

A light emitting diode is a device for performing a light emitting operation when a voltage of a turn-on voltage or more is applied thereto through anode and cathode terminals thereof. Generally, the turn-on voltage for causing the light emitting diode to emit light has a value much lower than the voltage of a common power source. Therefore, the light emitting diode has a disadvantage in that it cannot be used directly under the common AC power source of 110V or 220V. The operation of the light emitting diode using the common AC power source requires a voltage converter for lowering the supplied AC voltage. Accordingly, a driving circuit for the light emitting diode should be provided, which becomes one factor causing fabrication costs of an illuminating apparatus including the light emitting diode to be increased. Since a discrete driving circuit should be provided, the volume of the illuminating apparatus is increased and unnecessary heat is generated. In addition, there are problems such as improvement of a power factor for the supplied power.

To use the common AC power source in a state where a discrete voltage converting means is excluded, there has been suggested a method of constructing an array by connecting a plurality of light emitting diode chips in series to one another. To implement the light emitting diodes as an array, the light emitting diode chips should be formed into individual packages. Thus, a substrate separating process, a packaging process for a separated light emitting diode chip, and the like are required, and a mounting process of arranging the packages on an array substrate and a wiring process for forming wirings between electrodes of the packages are additionally required. Therefore, there are problems in that a processing time for constructing the array is increased, and fabrication costs of the array are increased.

Moreover, wire bonding is used for the wiring process of forming the array, and a molding layer for protecting bonding wires is additionally formed on an entire surface of the array. Accordingly, there is a problem in that a molding process of forming the molding layer is additionally required, resulting in increase in the complexity of processes. Particularly, in a case of application of a chip type with a lateral structure, the light-emitting performance of the light emitting diode chip is lowered, and the quality of the light emitting diode is deteriorated due to the generation of heat.

In order to solve the aforementioned problems, there has been proposed a light emitting diode chip array in which an array including a plurality of light emitting diode chips is fabricated as a single package.

In Korean Patent Laid-Open Publication No. 2007-0035745, a plurality of lateral type light emitting diode chips are electrically connected on a single substrate through metal wirings formed using an air bridge process. According to this laid-open publication, there is an advantage in that a discrete packaging process is not required for each of the individual chips, and an array is formed on a wafer level. However, the air bridge connection structure results in weak durability and the lateral type causes a problem of deterioration of the light-emitting performance or heat-dissipating performance.

In U.S. Pat. No. 6,573,537, a plurality of flip-chip type light emitting diodes are formed on a single substrate. However, n- and p-electrodes of each of the light emitting diodes are exposed to the outside in a state where the n- and p-electrodes are separated from each other. Therefore, a wiring process of connecting a plurality of electrodes to one another should be added in order to use a single power source. To this end, a submount substrate is used in the US patent. That is, the flip-chip type light emitting diodes should be mounted on a discrete submount substrate for wiring between the electrodes. At least two electrodes for electrical connection with another substrate should be formed on a back surface of the submount substrate. In the US patent, since the flip-chip type light emitting diodes are used, there is an advantage of improvement of the light-emitting performance and heat-dissipating performance. On the contrary, the use of the submount substrate causes increase in both fabrication costs and the thickness of a final product. In addition, there are further disadvantages of needs for an additional wiring process for the submount substrate and an additional process of mounting the submount substrate on a new substrate.

Korean Patent Laid-Open Publication No. 2008-0002161 discloses a configuration in which flip-chip type light emitting diodes are connected in series to one another. According to the laid-open patent publication, a packaging process on a chip basis is not required, and the use of the flip-chip type light emitting diodes exhibits an effect of improvement of the light-emitting performance and heat-dissipating performance. However, a discrete reflective layer is used in addition to wiring between n-type and p-type semiconductor layers, and interconnection wiring is used on the n-type electrode. Therefore, a plurality of patterned metal layers should be formed. To this end, various kinds of masks should be used, which becomes a problem. In addition, exfoliation or crack occurs due to a difference in thermal expansion coefficient between the n-electrode and the interconnection electrode, or the like, and therefore, there is a problem in that electrical contact therebetween is opened.

DISCLOSURE OF INVENTION

Technical Problem

An object of the present invention is to provide a flip-chip type light emitting diode array having an improved structure, and a method of forming the same.

Another object of the present invention is to provide a light emitting diode array that can be used without any submount substrate, and a method of forming the same.

A further object of the present invention is to provide a flip-chip type light emitting diode array that can prevent light loss without using an discrete reflective metal layer in addition to wires for connecting a plurality of light emitting diodes, and a method of forming the same.

A still further object of the present invention is to provide a flip-chip type light emitting diode array that can improve light extraction efficiency by reducing light loss, and a method of forming the same.

Other features and advantages of the present invention will be apparent and also better understood from the following description.

Technical Solution

A light emitting diode array according to an aspect of the present invention includes a growth substrate; a plurality of light emitting diodes arranged on the substrate, wherein each of the plurality of light emitting diodes has a first semiconductor layer, an active layer and a second semiconductor layer; and a plurality of upper electrodes arranged on the plurality of light emitting diodes and formed of an identical material, wherein each of the plurality of upper electrodes is electrically connected to the first semiconductor layer of a respective one of the light emitting diodes. At least one of the upper electrodes is electrically connected to the second semiconductor layer of an adjacent one of the light emitting diodes, and another of the upper electrodes is insulated from the second semiconductor layer of an adjacent one of the light emitting diodes.

Accordingly, it is possible to provide a flip-chip type light emitting diode array that can be driven under a high voltage and simplify a forming process thereof, without using any submount substrate.

The upper electrodes may include ohmic contact layers in ohmic contact with the first semiconductor layers. Since the upper electrodes include the ohmic contact layers, it is not necessary to form the ohmic contact layer and the upper electrode by using separate masks, and thus the forming process can be further simplified.

The ohmic contact layer may comprise a metallic material of Cr, Ni, Ti, Rh or Al; or ITO.

The upper electrodes may include reflective conductive layers. The reflective conductive layers may be positioned on the ohmic contact layers. The reflective conductive layers may comprise Al, Ag, Rh or Pt. Further, the upper electrodes may further include barrier layers for protecting the reflective conductive layers. The barrier layers may be formed into single- or multi-layered structures, and have a thickness of 300 to 5000 nm.

The light emitting diode array may further include a first interlayer insulating layers arranged between the light emitting diodes and the upper electrodes. The upper electrodes may be insulated from side surfaces of the light emitting diodes by the first interlayer insulating layer. The first interlayer insulating layer may cover the side surfaces of the light emitting diodes as well as regions between the light emitting diodes. The upper electrodes may be positioned on the first interlayer insulating layer and may cover most of the regions between the light emitting diodes. In a conventional case where linear wiring is used, the wiring hardly covers the regions between the light emitting diodes. On the contrary, the upper electrodes may cover at least 30%, at least 50% or even at least 90% of the regions between the light emitting diodes. However, since the upper electrodes are spaced apart from one another, the upper electrodes cover less than 100% of the regions between the light emitting diodes.

The upper electrodes may be formed to have relatively large areas in order to reduce resistance caused by the upper electrodes. Thus, it is possible to facilitate current distribution and to decrease a forward voltage of the light emitting diode array.

Further, the upper electrodes may construct, together with the first interlayer insulating layer, an omni-directional reflector. Alternatively, the first interlayer insulating layer may include a distributed Bragg reflector. Thus, the omni-directional reflector or the distributed Bragg reflector may further enhance the reflectance of light.

The light emitting diode array may further include lower electrodes respectively arranged on the second semiconductor layers of the light emitting diodes. The first interlayer insulating layer may expose a portion of the lower electrode on each of the light emitting diodes. The upper electrode(s) electrically connected to the second semiconductor layer of the adjacent light emitting diode may be connected to the exposed portion of the lower electrode through the first interlayer insulating layer. Each of the lower electrodes may include a reflective layer.

The light emitting diode array may further include a second interlayer insulating layer covering the upper electrodes. The second interlayer insulating layer may expose one of the lower electrodes and the upper electrode insulated from the second semiconductor layer of the adjacent light emitting diode.

Moreover, the light emitting diodes may be connected in series by the upper electrodes. At this time, the second interlayer insulating layer may expose lower and upper electrodes corresponding to light emitting diodes at both ends of the light emitting diodes connected in series.

The light emitting diode array may further include first and second pads positioned on the second interlayer insulating layer. The first pad may be connected to the lower electrode exposed through the second interlayer insulating layer, and the second pad may be connected to the upper electrode exposed through the second interlayer insulating layer. Accordingly, it is possible to provide a flip-chip type light emitting diode array that can be mounted on a printed circuit board or the like, using the first and second pads.

In some embodiments, each of the light emitting diodes may have a via hole for exposing the first semiconductor layer through the second semiconductor layer and the active layer. Each of the upper electrodes may be connected to the first semiconductor layer of a respective one of the light emitting diodes through the via hole.

Meanwhile, the upper electrodes may occupy at least 30% and less than 100% of the entire area of the light emitting diode array.

Each of the upper electrodes may be in the form of a plate or sheet having a ratio of length to width in a range of 1:3 to 3:1. Unlike a conventional linear wiring, since the upper electrodes are in the form of the plate or sheet, it is possible to facilitate current distribution and to decrease the forward voltage of the light emitting diode array.

At least one of the upper electrodes may have a length or width larger than that of a respective one of the light emitting diodes. Thus, the upper electrode can cover the region between the light emitting diodes, and can reflect light generated in the active layer toward the substrate.

A method of forming a light emitting diode array according to another aspect of the present invention include forming a plurality of light emitting diodes, wherein each of the plurality of light emitting diodes has a first semiconductor layer, an active layer and a second semiconductor layer on a growth substrate. Each of the plurality of light emitting diodes has the

first semiconductor layer exposed by removing the second semiconductor layer and the active layer. Subsequently, a first interlayer insulating layer for covering the light emitting diodes is formed. The first interlayer insulating layer exposes the exposed first semiconductor layers and has openings positioned on the second semiconductor layer of each of the light emitting diodes. In addition, a plurality of upper electrodes are formed from an identical material on the first interlayer insulating layer. Each of the upper electrodes is connected to the first semiconductor layer of a respective one of the light emitting diodes. Furthermore, at least one of the upper electrodes is electrically connected to the second semiconductor layer of an adjacent one of the light emitting diodes through the opening of the first interlayer insulating layer, and another of the upper electrodes is insulated from the second semiconductor layer of an adjacent one of the light emitting diodes.

Accordingly, it is possible to form a flip-chip type light emitting diode array in which the light emitting diodes can be electrically connected using the upper electrodes. Therefore, it is not necessary to use a submount substrate. The upper electrode may include an ohmic contact layer, and thus it is not necessary to form a separate ohmic contact layer on the first semiconductor layer of each of the light emitting diodes.

Further, each of the upper electrodes may include a reflective conductive layer. Since the upper electrode includes the reflective conductive layer, it is possible to reduce light loss of the light emitting diode array.

Meanwhile, the method may further include forming lower electrodes on the second semiconductor layers of the respective light emitting diodes before the first interlayer insulating layer is formed. The lower electrodes may be formed before or after forming a plurality of light emitting diodes separated each other, which are formed by patterning the first semiconductor layer, the active layer and the second semiconductor layer.

The method may further include forming a second interlayer insulating layer on the upper electrodes. The second interlayer insulating layer may expose one of the lower electrodes and the other upper electrode insulated from the second semiconductor layer of the adjacent light emitting diode.

The method may further include forming first and second pads on the second interlayer insulating layer. The first pad may be connected to the lower electrode, and the second pad may be connected to the upper electrode.

Meanwhile, the method may further include cutting the growth substrate into individual units. The upper electrodes occupy at least 30% and less than 100% of the area of the light emitting diode array of each of the cut individual units.

In some embodiments, the first interlayer insulating layer may be formed as a distributed Bragg reflector. In other embodiments, the first interlayer insulating layer may construct, together with the upper electrode, an omni-directional reflector.

Advantageous Effects

According to embodiments of the present invention, it is possible to provide a flip-chip type light emitting diode array having an improved structure. In particular, it is possible to provide a light emitting diode array on a wafer level, which can be driven at a high voltage. Further, the light emitting diode array may not require a submount substrate. Since the upper electrode can include an ohmic contact layer, it is not necessary to form a discrete ohmic contact layer.

In addition, the upper electrodes include reflective conductive layers. Further, since the upper electrodes cover side surfaces of the light emitting diodes and most of the regions between the light emitting diodes, the upper electrodes can be used to reflect light. Thus, it is possible to reduce a loss of light generated in the regions between the light emitting diodes. Further, it is not necessary to additionally form a discrete reflective metal layer for reflecting light, in addition to the upper electrodes (wirings).

Furthermore, the upper electrodes are made in the form of a plate or sheet having a wide area, thereby improve current distribution performance and decreasing a forward voltage at an identical current while using an identical number of light emitting diodes.

Moreover, since the first and second pads occupy a relatively large area, it is possible to easily and firmly mount the light emitting diode array on a printed circuit board or the like.

DESCRIPTION OF DRAWINGS

FIGS. **1** and **2** are plan and sectional views showing that a plurality of via holes are formed in a laminated structure according to an embodiment of the present invention.

FIGS. **3** and **4** are plan and sectional views showing that lower electrodes are formed on a second semiconductor layer of FIG. **1**.

FIG. **5** is a plan view showing a state where cell regions are separated with respect to the structure of FIG. **3**.

FIG. **6** is a sectional view taken along line A**1**-A**2** in the plan view of FIG. **5**.

FIG. **7** is a perspective view of the structure in the plan view of FIG. **5**.

FIG. **8** is a plan view showing that a first interlayer insulating layer is formed on an entire surface of the structure of FIGS. **5** to **7**, and portions of a first semiconductor layer and the lower electrodes are exposed in each of the cell regions.

FIGS. **9** to **12** are sectional views taken along specific lines in the plan view of FIG. **8**.

FIG. **13** is a plan view showing that upper electrodes are formed on the structure illustrated in FIGS. **8** to **12**.

FIGS. **14** to **17** are sectional views taken along specific lines in the plan view of FIG. **13**.

FIG. **18** is a perspective view of the structure in the plan view of FIG. **13**.

FIG. **19** is an equivalent circuit diagram obtained by modeling the structure of FIGS. **13** to **18** according to an embodiment of the present invention.

FIG. **20** is a plan view showing that a second interlayer insulating layer is applied on an entire surface of the structure of FIG. **13**, a portion of a first electrode in a first cell region is exposed, and a portion of a fourth lower electrode in a fourth cell region is exposed.

FIGS. **21** to **24** are sectional views taken along specific lines in the plan view of FIG. **20**.

FIG. **25** is a plan view showing that first and second pads are formed in the structure of FIG. **20**.

FIGS. **26** to **29** are sectional views taken along specific lines in the plan view of FIG. **25**.

FIG. **30** is a perspective view taken along line C**2**-C**3** in the plan view of FIG. **25**.

FIG. **31** is a circuit diagram obtained by modeling a connection of ten light emitting diodes in series according to an embodiment of the present invention.

FIG. **32** is a circuit diagram obtained by modeling an array having light emitting diodes connected in series/parallel according to an embodiment of the present invention.

(Description of Reference Numerals)

100: substrate	111, 112, 113, 114: first semiconductor layer
121, 122, 123, 124: active layer	131, 132, 133, 134: second semiconductor layer
140: via hole	151: first lower electrode
152: second lower electrode	153: third lower electrode
154: fourth lower electrode	161: first cell region
162: second cell region	163: third cell region
164: fourth cell region	170: first interlayer insulating layer
181: first upper electrode	182: second upper electrode
183: third upper electrode	184: fourth upper electrode
190: second interlayer insulating layer	
210: first pad	220: second pad

MODE FOR INVENTION

Hereinafter, exemplary embodiments of the present invention will be described in detail with reference to the accompanying drawings, in order to more specifically describe the present invention. However, the present invention is not limited to the following embodiments described herein but may be implemented in other forms.

In these embodiments, it will be understood that the term "first", "second", "third" or the like does not impose any limitation on components but are only used to distinguish the components.

FIGS. **1** and **2** are plan and sectional views showing that a plurality of via holes are formed in a laminated structure according to an embodiment of the present invention.

In particular, FIG. **2** is a sectional view taken along line A**1**-A**2** in the plan view of FIG. **1**.

Referring to FIGS. **1** and **2**, a first semiconductor layer **110**, an active layer **120** and a second semiconductor layer **130** are formed on a substrate **100**, and via holes **140** are formed to allow a surface of the semiconductor layer **110** to be exposed therethrough.

The substrate **100** comprises a material such as sapphire, silicon carbide or GaN. Any material may be used for the substrate **100** as long as it can induce the growth of a thin film to be formed on the substrate **100**. The first semiconductor layer **110** may have n-type conductivity. The active layer **120** may have a multiple quantum well structure, and the second semiconductor layer **130** is formed on the active layer **120**. When the first semiconductor layer **110** has the n-type conductivity, the second semiconductor layer **130** has p-type conductivity. A buffer layer (not shown) may be further formed between the substrate **100** and the first semiconductor layer **110** so as to facilitate single crystalline growth of the first semiconductor layer **110**.

Subsequently, selective etching is performed on the structure formed with up to the second semiconductor layer **130**, and a plurality of via holes **140** are formed. Portions of the lower first semiconductor layer **110** are exposed through the via holes **140**. The via holes **140** may be formed through a conventional etching process. For example, a photoresist is applied, and portions of the photoresist on regions where the via holes will be formed are then removed through a conventional patterning process to form a photoresist pattern. Thereafter, an etching process is performed by using the photoresist pattern as an etching mask. The etching process is performed until the portions of the first semiconductor layer **110** are exposed. After the etching process, the remaining photoresist pattern is removed.

The shape and number of the via holes **140** may be variously changed.

FIGS. **3** and **4** are plan and sectional views showing that lower electrodes are formed on the second semiconductor layer of FIG. **1**. Particularly, FIG. **4** is a sectional view taken along line A**1**-A**2** in the plan view of FIG. **3**.

Referring to FIGS. **3** and **4**, the lower electrodes **151**, **152**, **153** and **154** are formed in regions except the via holes **140**, and a plurality of cell regions **161**, **162**, **163** and **164** may be defined by the formation of the lower electrodes **151**, **152**, **153** and **154**. The lower electrodes **151**, **152**, **153** and **154** may be formed by employing a lift-off process used upon formation of a metal electrode. For example, a photoresist is formed in separating regions excluding the virtual cell regions **161**, **162**, **163** and **164** and in the regions in which the via holes **140** are formed, and a metal layer is formed through conventional thermal deposition or the like. Subsequently, the photoresist is removed, thereby forming the lower electrodes **151**, **152**, **153** and **154** on the second semiconductor layer **130**. Any material may be employed for the lower electrodes **151**, **152**, **153** and **154** as long as it is a metallic material capable of being in ohmic contact with the second semiconductor layer **130**. The lower electrodes **151**, **152**, **153** and **154** may include a reflective layer of a material such as Al, Ag, Rh or Pt. For example, the lower electrodes **151**, **152**, **153** and **154** may comprise Ni, Cr or Ti, and may be composed of a composite metal layer of Ti/Al/Ni/Au.

In FIGS. **3** and **4**, the regions in which the four lower electrodes **151**, **152**, **153** and **154** are formed define four cell regions **161**, **162**, **163** and **164**, respectively. The second semiconductor layer **130** is exposed in spaces among the cell regions **161**, **162**, **163** and **164**. The number of the cell regions may correspond to that of light emitting diodes included in an array to be formed. Therefore, the number of the cell regions **161**, **162**, **163** and **164** may be variously changed.

Although FIG. **4** shows that the lower electrode **151**, **152**, **153** or **154** is separated in the same cell region **161**, **162**, **163** or **164**, this is a phenomenon occurring as line A**1**-A**2** transverses the via holes **140**. As can be seen in FIG. **3**, the lower electrode **151**, **152**, **153** or **154** formed in the same cell region **161**, **162**, **163** or **164** is physically continuous. Thus, the lower electrode **151**, **152**, **153** or **154** formed in the same cell region is in an electrically short-circuited state even though the via holes **140** are formed therein.

FIG. **5** is a plan view showing a state where cell regions are separated with respect to the structure of FIG. **3**, FIG. **6** is a sectional view taken along line A**1**-A**2** in the plan view of FIG. **5**, and FIG. **7** is a perspective view of the structure in the plan view of FIG. **5**.

Referring to FIGS. **5**, **6** and **7**, mesa-etched regions are formed through mesa etching for the spaces among the four cell regions **161**, **162**, **163** and **164**. The substrate **100** is exposed in the mesa-etched regions formed through the mesa etching. Thus, the four cell regions **161**, **162**, **163** and **164** are electrically completely separated from one another. If a buffer layer is interposed between the substrate **100** and the first semiconductor layer **110** in FIGS. **1** to **4**, the buffer layer may remain even in the separation process of the cell regions **161**, **162**, **163** and **164**. However, in order to completely separate the cell regions **161**, **162**, **163** and **164** from one another, the buffer layer between adjacent ones of the cell regions **161**, **162**, **163** and **164** may be removed through the mesa etching.

With the separation process between adjacent ones of the cell regions **161**, **162**, **163** and **164**, first semiconductor layers **111**, **112**, **113** and **114**, active layers **121**, **122**, **123** and **124**, second semiconductor layers **131**, **132**, **133** and **134** and lower electrodes **151**, **152**, **153** and **154** are independently formed in the cell regions **161**, **162**, **163** and **164**, respectively. Thus, the first lower electrode **151** is exposed in the first cell

region **161**, and the first semiconductor layer **111** is exposed through the via holes **140**. The second lower electrode **152** is exposed in the second cell region **162**, and the first semiconductor layer **112** is exposed through the via holes **140**. Similarly, the third lower electrode **153** and the first semiconductor layer **113** are exposed in the third cell region **163**, and the fourth lower electrode **154** and the first semiconductor layer **114** are exposed in the fourth cell region **164**.

In the present invention, the light emitting diode refers to a structure in which the first semiconductor layer **111**, **112**, **113** or **114**, the active layer **121**, **122**, **123** or **124** and the second semiconductor layer **131**, **132**, **133** or **134** are laminated, respectively. Thus, one light emitting diode is formed in one cell region. When the light emitting diode is modeled such that the first semiconductor layer **111**, **112**, **113** or **114** has n-type conductivity and the second semiconductor layer **131**, **132**, **133** or **134** has p-type conductivity, the lower electrode **151**, **152**, **153** or **154** formed on the second semiconductor layer **131**, **132**, **133** or **134** may be referred to as an anode electrode of the light emitting diode.

FIG. **8** is a plan view showing that a first interlayer insulating layer is formed on an entire surface of the structure of FIGS. **5** to **7**, and portions of a first semiconductor layer and the lower electrodes are exposed in each of the cell regions.

Moreover, FIGS. **9** to **12** are sectional views taken along specific lines in the plan view of FIG. **8**. Particularly, FIG. **9** is a sectional view taken along line B**1**-B**2** in the plan view of FIG. **8**, FIG. **10** is a sectional view taken along line C**1**-C**2** in the plan view of FIG. **8**, FIG. **11** is a sectional view taken along line D**1**-D**2** in the plan view of FIG. **8**, and FIG. **12** is a sectional view taken along line E**1**-E**2** in the plan view of FIG. **8**.

First, a first interlayer insulating layer **170** is formed with respect to the structure of FIGS. **5** to **7**. Moreover, portions of the lower electrodes **151**, **152**, **153** and **154** and of the first semiconductor layers **111**, **112**, **113** and **114** under the via holes are exposed by means of patterning.

For example, in the first cell region **161**, two pre-formed via holes are opened so that portions of the first semiconductor layer **111** are exposed, and a portion of the first lower electrode **151** formed on the pre-formed second semiconductor layer **131** is exposed. In the second cell region **162**, portions of the first semiconductor layer **112** are exposed through the pre-formed via holes, and a portion of the second lower electrode **152** is exposed by means of etching for a portion of the first interlayer insulating layer **170**. In the third cell region **163**, portions of the first semiconductor layer **113** are exposed through the via holes, and a portion of the third lower electrode **153** is exposed by means of etching for a portion of the first interlayer insulating layer **170**. In the fourth cell region **164**, portions of the first semiconductor layer **114** are exposed through the via holes, and a portion of the fourth lower electrode **154** is exposed by means of etching for a portion of the first interlayer insulating layer **170**.

As a result, in FIGS. **8** to **12**, the first interlayer insulating layer **170** is formed on the entire surface of the substrate, and the portions of the first semiconductor layers **111**, **112**, **113** and **114** under the via holes and the portions of the lower electrodes **151**, **152**, **153** and **154** on the second semiconductor layers **131**, **132**, **133** and **134** are exposed in each of the cell regions **161**, **162**, **163** and **164** by means of selective etching. That is, in the respective cell regions **161**, **162**, **163** and **164**, the portions of the first semiconductor layers **111**, **112**, **113** and **114** are exposed through the via holes previously formed in the preceding process, and the portions of the lower electrodes **151**, **152**, **153** and **154** are also exposed. The remaining region is shielded by the first interlayer insulating layer **170**.

The first interlayer insulating layer **170** may be formed of an insulating material having a light transmittance. For example, the first interlayer insulating layer may comprise SiO_2. Alternatively, the first interlayer insulating layer **170** may be formed as a distributed Bragg reflector in which material layers having different refractive indices are laminated. For example, the first interlayer insulating layer **170** can be formed by repetitively laminating SiO_2/TiO_2, thereby reflecting light generated from the active layer.

FIG. **13** is a plan view showing that upper electrodes are formed on the structure illustrated in FIGS. **8** to **12**, and FIGS. **14** to **17** are sectional views taken along specific lines in the plan view of FIG. **13**. Particularly, FIG. **14** is a sectional view taken along line B**1**-B**2** in the plan view of FIG. **13**, FIG. **15** is a sectional view taken along line C**1**-C**2** in the plan view of FIG. **13**, FIG. **16** is a sectional view taken along line D**1**-D**2** in the plan view of FIG. **13**, and FIG. **17** is a sectional view taken along line E**1**-E**2** in the plan view of FIG. **13**.

Referring to FIG. **13**, upper electrodes **181**, **182**, **183** and **184** are formed. The upper electrodes **181**, **182**, **183** and **184** are formed as four discrete regions. For example, the first upper electrode **181** is formed over the first cell region **161** and a portion of the second cell region **162**. The second upper electrode **182** is formed over a portion of the second cell region **162** and a portion of the third cell region **163**. The third upper electrode **183** is formed over a portion of the third cell region **163** and a portion of the fourth cell region **164**. The fourth upper electrode **184** is formed in a portion of the fourth cell region **164**. Thus, each of the upper electrodes **181**, **182**, **183** and **184** is formed while shielding spaces between adjacent ones of the cell regions. The upper electrodes **181**, **182**, **183** and **184** may cover no less than 30%, even no less than 50%, or no less than 90% of the spaces between the adjacent cell regions. However, since the upper electrodes **181**, **182**, **183** and **184** are spaced apart from one another, the upper electrodes **181**, **182**, **183** and **184** cover less than 100% of regions between adjacent ones of light emitting diodes.

The entire of the upper electrodes **181**, **182**, **183** and **184** may occupy no less than 30%, no less than 50%, no less than 70%, no less than 80% or no less than 90% of the entire area of the light emitting diode array. However, since the upper electrodes **181**, **182**, **183** and **184** are spaced apart from one another, they occupy less than 100% of the entire area of the light emitting diode array. Each of the upper electrodes **181**, **182**, **183** and **184** has the shape of a plate or sheet having a ratio of length and width ranging from 1:3 to 3:1. Further, at least one of the upper electrodes **181**, **182**, **183** and **184** has a length or width greater than that of a corresponding light emitting diode (cell region).

Referring to FIG. **14**, the first upper electrode **181** is formed on the first interlayer insulating layer **170** in the first cell region **161**, and is formed on portions of the first semiconductor layer **111** opened through the via holes. In addition, the first upper electrode **181** allows a portion of the first lower electrode **151** to be opened in the first cell region **161** and is formed on a portion of the second lower electrode **152** exposed in the second cell region **162**.

The second upper electrode **182** is formed on portions of the first semiconductor layer **112** exposed through the via holes in the second cell region **162** in a state in which the second upper electrode **182** is physically separated from the first upper electrode **181**. In addition, the second upper electrode **182** is formed on the first interlayer insulating layer **170**.

In FIG. **14**, the first upper electrode **181** electrically connects the first semiconductor layer **111** in the first cell region **161** to the second semiconductor layer **132** in the second cell region **162**. Despite of the presence of the via holes, the

second lower electrode **152** in the second cell region **162** is entirely in an electrically short-circuited state in one cell region. Thus, the first semiconductor layer **111** in the first cell region **161** is electrically connected to the second semiconductor layer **132** in the second cell region **162** through the second lower electrode **152**.

In FIG. **15**, the second upper electrode **182** is formed on portions of the first semiconductor layer **112** exposed through the via holes in the second cell region **162**, and is formed to extend to the third lower electrode **153** in the third cell region **163**. The third upper electrode **183** physically separated from the second upper electrode **182** is also formed on portions of the first semiconductor layer **113** exposed through the via holes in the third cell region **163**.

In FIG. **15**, the second upper electrode **182** is electrically connected to the portions of the first semiconductor layer **112** through the via holes in the second cell region **162**, and is electrically connected to the third lower electrode **153** in the third cell region **163**. Thus, the first semiconductor layer **112** in the second cell region **162** can maintain the same potential as the second semiconductor layer **133** in the third cell region **163**.

Referring to FIG. **16**, the third upper electrode **183** is formed on portions of the first semiconductor layer **113** exposed through the via holes in the third cell region **163**, and is formed to extend to the fourth lower electrode **154** in the fourth cell region **164**. Thus, the first semiconductor layer **113** in the third cell region **163** is electrically connected to the second semiconductor layer **134** in the fourth cell region **164**. The fourth upper electrode **184** physically separated from the third upper electrode **183** is electrically connected to the portions of the first semiconductor layer **114** exposed through the via holes in the fourth cell region **164**.

Referring to FIG. **17**, the fourth upper electrode **184** is formed on portions of the first semiconductor layer **114** exposed through the via holes in the fourth cell region **164**. The first upper electrode **181** physically separated from the fourth upper electrode **184** is formed on portions of the first semiconductor layer **111** exposed through the via holes in the first cell region **161**, and allows a portion of the first lower electrode **151** to be exposed in the first cell region **161**.

The contents disclosed in FIGS. **13** to **17** will be summarized below. The first semiconductor layer **111** in the first cell region **161** and the second semiconductor layer **132** in the second cell region **162** establish the same potential through the first upper electrode **181**. The first semiconductor layer **112** in the second cell region **162** and the second semiconductor layer **133** in the third cell region **163** establish the same potential through the second upper electrode **182**. The first semiconductor layer **113** in the third cell region **163** establish the same potential as the second semiconductor layer **134** in the fourth cell region **164** through the third upper electrode **183**. The first lower electrode **151** electrically connected to the second semiconductor layer **131** in the first cell region **161** is exposed.

Of course, the same potential is established by assuming ideal electrical connection in a state where resistances of the upper electrodes **181**, **182**, **183** and **184** and contact resistances between the upper electrodes **181**, **182**, **183** and **184** and the lower electrodes **151**, **152**, **153** and **154** are neglected. Thus, in the operation of an actual device, a voltage drop may be sometimes caused by resistance components of the upper electrodes **181**, **182**, **183** and **184** and the lower electrodes **151**, **152**, **153** and **154**, which are kinds of metal wires.

Meanwhile, the upper electrodes **181**, **182**, **183** and **184** may include a reflective conductive layer **180***b*. The reflective conductive layer **180***b* may comprise Al, Ag, Rh, Pt or a combination thereof. The upper electrodes **181**, **182**, **183** and **184** including the reflective conductive layer **180***b* may reflect light, which is generated from the active layers **121**, **122**, **123** and **124** in the respective cell regions **161**, **162**, **163** and **164**, toward the substrate **100**. Further, the upper electrodes **181**, **182**, **183** and **184** may construct, together with the first interlayer insulating layer **170**, omni-directional reflectors. Meanwhile, even when the first interlayer insulating layer **170** is formed as the distributed Bragg reflector, the upper electrodes **181**, **182**, **183** and **184** including the reflective conductive layer **180***b* can also improve light reflectivity.

The upper electrodes **181**, **182**, **183** and **184** may also include an ohmic contact layer **180***a*. The reflective conductive layer **180***b* may be positioned on the ohmic contact layer **180***a*. The ohmic contact layer **180***a* comprises a material, such as Ni, Cr, Ti, Rh, Al or combination thereof, that can be in ohmic contact with the first semiconductor layers **111**, **112**, **113** and **114** and the lower electrodes **151**, **152**, **153** and **154**. However, the ohmic contact layer **180***a* is not limited thereto, and any material may be used for the ohmic contact layer **180***a* as long as it is a material that can be in ohmic contact with the lower electrodes **151**, **152**, **153** and **154** made of a metallic material while being in ohmic contact with the first semiconductor layers **111**, **112**, **113** and **114**. A layer of conductive oxide such as ITO may be used.

The light generated from the active layers **121**, **122**, **123** and **124** in the respective cell regions **161**, **162**, **163** and **164** may be reflected from the lower electrodes **151**, **152**, **153** and **154** toward the substrate **100**. In addition, light transmitted through the spaces between the adjacent ones of the cell regions **161**, **162**, **163** and **164** is reflected by the first interlayer insulating layer **170** shielding the spaces between the adjacent ones of the cell regions **161**, **162**, **163** and **164** and/or the upper electrodes **181**, **182**, **183** and **184**. The light L generated from the active layers **121**, **122**, **123** and **124** and directed to the via holes or the spaces between the adjacent ones of the cell regions **161**, **162**, **163** and **164** is reflected by the first interlayer insulating layer **170** disposed on sidewalls of the via holes or spaces and/or by the upper electrodes **181**, **182**, **183** and **184** having the reflective conductive layer **180***b*, so that the light can be extracted to the outside through the substrate **100**. Accordingly, it is possible to reduce light loss, thereby improving light extraction efficiency.

To this end, it is preferable that the upper electrodes **181**, **182**, **183** and **184** occupy a large area in the light emitting diode array. For example, the upper electrodes **181**, **182**, **183** and **184** may cover no less than 70%, no less than 80% or even no less than 90% of the entire area of the light emitting diode array. An interval between the upper electrodes **181**, **182**, **183** and **184** may be in a range of about 1 to 100 μm. More preferably, the interval between the upper electrodes **181**, **182**, **183** and **184** may be 5 to 15 μm. Accordingly, it is possible to prevent light leakage in the via holes or the spaces between the adjacent ones of the cell regions **161**, **162**, **163** and **164**.

The upper electrodes **181**, **182**, **183** and **184** may further include a barrier layer **180***c* disposed on the reflective conductive layer **180***b*. The barrier layer **180***c* may comprise Ti, Ni, Cr, Pt, TiW, W, Mo or a combination thereof. The barrier layer **180***c* can prevent the reflective conductive layer **180***b* from being damaged during a subsequent etching or cleaning process. The barrier layer **180***c* may be formed as a single- or multi-layered structure and to have a thickness ranging from 300 to 5000 nm.

If the first semiconductor layers **111**, **112**, **113** and **114** have n-type conductivity and the second semiconductor layers **131**, **132**, **133** and **134** have p-type conductivity, each of

the upper electrodes may be modeled as a cathode electrode of the light emitting diode, and simultaneously as wiring for connecting the cathode electrode of the light emitting diode to the lower electrode that is an anode electrode of a light emitting diode formed in an adjacent cell region. That is, in the light emitting diode formed in the cell region, the upper electrode may be modeled to form a cathode electrode and simultaneously to be wiring for electrically connecting the cathode electrode of the light emitting diode to an anode electrode of a light emitting diode in an adjacent cell region.

FIG. **18** is a perspective view of the structure in the plan view of FIG. **13**.

Referring to FIG. **18**, the first to third upper electrodes **181** to **183** are formed over at least two cell regions. The space between adjacent cell regions is shielded. The upper electrodes allow light, which may be leaked between adjacent cell regions, to be reflected through the substrate, and are electrically connected to the first semiconductor layer in each cell region. The upper electrodes are electrically connected to the second semiconductor layer in an adjacent cell region.

FIG. **19** is an equivalent circuit diagram obtained by modeling the structure of FIGS. **13** to **18** according to an embodiment of the present invention.

Referring to FIG. **19**, four light emitting diodes D**1**, D**2**, D**3** and D**4** and a wiring relationship among the light emitting diodes are shown.

The first light emitting diode D**1** is formed in the first cell region **161**, the second light emitting diode D**2** is formed in the second cell region **162**, the third light emitting diode D**3** is formed in the third cell region **163**, and the fourth light emitting diode D**4** is formed in the fourth cell region **164**. The first semiconductor layers **111**, **112**, **113** and **114** in the cell regions **161**, **162**, **163** and **164** are modeled as n-type semiconductors, and the second semiconductor layers **131**, **132**, **133** and **134** are modeled as p-type semiconductors.

The first upper electrode **181** is electrically connected to the first semiconductor layer **111** in the first cell region **161** and extends to the second cell region **162** so as to be electrically connected to the second semiconductor layer **132** in the second cell region **162**. Thus, the first upper electrode **181** is modeled as wiring for connecting a cathode terminal of the first light emitting diode D**1** to an anode electrode of the second light emitting diode D**2**.

The second upper electrode **182** is modeled as wiring for connection between a cathode terminal of the second light emitting diode D**2** and an anode terminal of the third light emitting diode D**3**. The third upper electrode **183** is modeled as wiring for connection between a cathode electrode of the third light emitting diode D**3** and an anode terminal of the fourth light emitting diode D**4**. The fourth upper electrode **184** is modeled as wiring for forming a cathode electrode of the fourth light emitting diode D**4**.

Thus, the anode terminal of the first light emitting diode D**1** and the cathode terminal of the fourth light emitting diode D**4** are in an electrically opened state with respect to an external power source, and the other light emitting diodes D**2** and D**3** are electrically connected in series.

FIG. **20** is a plan view showing that a second interlayer insulating layer is applied on an entire surface of the structure of FIG. **13**, a portion of the first electrode in the first cell region is exposed, and a portion of the fourth lower electrode in the fourth cell region is exposed.

FIG. **21** is a sectional view taken along line B**1**-B**2** in the plan view of FIG. **20**, FIG. **22** is a sectional view taken along line C**1**-C**2** in the plan view of FIG. **20**, FIG. **23** is a sectional view taken along line D**1**-D**2** in the plan view of FIG. **20**, and FIG. **24** is a sectional view taken along line E**1**-E**2** in the plan view of FIG. **20**.

Referring to FIG. **21**, in the first cell region **161**, portions of the first lower electrode **151** electrically connected to the second semiconductor layer **131** are opened. The remaining portions in the first cell region are covered with the second interlayer insulating layer **190** that is also over the second cell region **162**.

Referring to FIG. **22**, the second and third cell regions **162** and **163** are completely covered with the second interlayer insulating layer **190**.

Referring to FIGS. **23** and **24**, portions of the fourth upper electrode **184** in the fourth cell region **164** are exposed, and portions of the first lower electrode **151** in the first cell region **161** are exposed.

The second interlayer insulating layer **190** is selected from an insulation material capable of protecting an underlying film from an external environment. In particular, the second interlayer insulating layer may comprise SiN or the like that has an insulation property and can block a change in temperature or humidity.

In FIGS. **20** to **24**, the second interlayer insulating layer **190** is applied to the entire structure formed on the substrate, and also exposes a portion of the first lower electrode **151** in the first cell region **161** and exposes the fourth upper electrode **184** in the fourth cell region **164**.

FIG. **25** is a plan view showing that first and second pads are formed in the structure of FIG. **20**.

Referring to FIG. **25**, the first pad **210** may be formed over the first and second cell regions **161** and **162**. Accordingly, the first pad **210** can be electrically connected to the first lower electrode **151** in the first cell region **161**, which is exposed in FIG. **20**.

Moreover, the second pad **220** is formed to be spaced apart from the first pad **210** at a predetermined distance, and may be formed over the third and fourth cell regions **163** and **164**. The second pad **220** is electrically connected to the fourth upper electrode **184** in the fourth cell region **164**, which is exposed in FIG. **20**.

FIG. **26** is a sectional view taken along line B**1**-B**2** in the plan view of FIG. **25**, FIG. **27** is a sectional view taken along line C**1**-C**2** in the plan view of FIG. **25**, FIG. **28** is a sectional view taken along line D**1**-D**2** in the plan view of FIG. **25**, and FIG. **29** is a sectional view taken along line E**1**-E**2** in the plan view of FIG. **25**.

Referring to FIG. **26**, the first pad **210** is formed over the first and second cell regions **161** and **162**. The first pad **210** is formed on the first lower electrode **151** exposed in the first cell region **161**, and on the second interlayer insulating layer **190** in the other cell regions. Thus, the first pad **210** is electrically connected to the second semiconductor layer **131** in the first cell region **161** through the first lower electrode **151**.

Referring to FIG. **27**, the first pad **210** is formed in the second cell region **162**, and the second pad **220** is formed in the third cell region **163** to be spaced apart from the first pad **210**. The electrical contact of the first or second pad **210** or **220** with the lower or upper electrode is blocked in the second and third cell regions **162** and **163**.

Referring to FIG. **28**, the second pad **220** is formed over the third and fourth cell regions **163** and **164**. Particularly, the second pad **220** is electrically connected to the fourth upper electrode **184** opened in the fourth cell region **164**. Thus, the second pad **220** is electrically connected to the first semiconductor layer **114** in the fourth cell region **164**.

Referring to FIG. **29**, the second pad **220** is formed in the fourth cell region **164**, and the first pad **210** is formed to be

spaced apart from the second pad **220** in the first cell region **161**. The first pad **210** is formed on the first lower electrode **151** in the first cell region **161** and electrically connected to the second semiconductor layer **131**.

FIG. **30** is a perspective view taken along line C**2**-C**3** in the plan view of FIG. **25**.

Referring to FIG. **30**, the first semiconductor layer **113** in the third cell region **163** is electrically connected to the third upper electrode **183**. The third upper electrode **183** shields the space between the third and fourth cell regions **163** and **164** and is electrically connected to the fourth lower electrode **154** in the fourth cell region **164**. The first and second pads **210** and **220** are spaced apart from each other and formed on the second interlayer insulating layer **190**. Of course, as described above, the first pad **210** is electrically connected to the second semiconductor layer **131** in the first cell region **161**, and the second pad **220** is electrically connected to the first semiconductor layer **114** in the fourth cell region **164**.

Referring to the modeling of FIG. **19**, the first semiconductor layers **111**, **112**, **113** and **114** in the respective cell regions are modeled as n-type semiconductors, and the second semiconductor layers **131**, **132**, **133** and **134** in the respective cell regions are modeled as p-type semiconductors. The first lower electrode **151** formed on the second semiconductor layer **131** in the first cell region **161** is modeled as the anode electrode of the first light emitting diode D**1**. Thus, the first pad **210** can be modeled as wiring connected to the anode electrode of the first light emitting diode D**1**. The fourth upper electrode **184** electrically connected to the first semiconductor layer **114** in the fourth cell region **164** is modeled as the cathode electrode of the fourth light emitting diode D**4**. Thus, the second pad **220** can be modeled as wiring connected to the cathode electrode of the fourth light emitting diode D**4**.

Accordingly, an array structure in which the four light emitting diodes D**1** to D**4** are connected in series formed, and electrical connection thereof to the outside is achieved through the two pads **210** and **220** formed on the single substrate **100**.

In the present invention, there is shown that the four light emitting diodes are formed while being separated from one another and an anode terminal of one of the light emitting diodes is electrically connected to a cathode terminal of another of the light emitting diodes through the lower and upper electrodes. However, the four light emitting diodes in this embodiment are merely an example, and a various number of light emitting diodes may be formed.

FIG. **31** is a circuit diagram obtained by modeling a connection of ten light emitting diodes in series according to an embodiment of the present invention.

Referring to FIG. **31**, ten cell regions **301** to **310** are defined using the process shown in FIG. **5**. A first semiconductor layer, an active layer, a second semiconductor layer and a lower electrode in each of the cell regions **301** to **310** are separated from those in other cell regions. The respective lower electrodes are formed on the second semiconductor layers so as to form anode electrodes of light emitting diodes D**1** to D**10**.

Subsequently, a first interlayer insulating layer and first to tenth upper electrodes **181**, **182**, **183**, **184**, **185**, **186**, **187**, **188**, **189** and **189'** are formed using the processes shown in FIGS. **6** to **17**. The upper electrodes **181**, **182**, **183**, **184**, **185**, **186**, **187**, **188**, **189** and **189'** shield the space between adjacent cell regions. The first to ninth upper electrodes **181**, **182**, **183**, **184**, **185**, **186**, **187**, **188** and **189** serve as wiring for achieving electrical connection between an anode electrode of one of a pair of adjacent light emitting diodes and a first semiconductor layer of the other of the pair of adjacent light emitting diodes. The tenth upper electrode **189'** is electrically connected to the first semiconductor layer of the light emitting diode D**10**.

Furthermore, a second interlayer insulating layer is formed using the processes shown in FIGS. **20** to **29**. The lower electrode of the first light emitting diode D**1** connected to a positive power voltage V+ on a current path is exposed, and the upper electrode of the tenth light emitting diode D**10** connected to a negative power voltage V− on the current path is opened. Then, a first pad **320** is formed and connected to the anode terminal of the first light emitting diode D**1**, and a second pad **330** is formed and connected to a cathode terminal of the tenth light emitting diode D**10**.

The other light emitting diodes are connected in series/parallel so as to form an array.

FIG. **32** is a circuit diagram obtained by modeling an array having light emitting diodes connected in series/parallel according to an embodiment of the present invention.

Referring to FIG. **32**, a plurality of light emitting diodes D**1** to D**8** are connected in series and/or in parallel to one another. The light emitting diodes D**1** to D**8** are formed independently of one another through the definitions of cell regions **401** to **408**. As described above, an anode electrode of each of the light emitting diode D**1** to D**8** is formed through a lower electrode. Wiring between a cathode electrode of each of the light emitting diodes D**1** to D**8** and the anode electrode of an adjacent light emitting diode is made by forming an upper electrode and performing an appropriate wiring process. However, the lower electrode is formed on a second semiconductor layer, and the upper electrode is formed to shield the space between adjacent cell regions.

Finally, a first pad **410** supplied with a positive power voltage V+ is electrically connected to the lower electrode formed on the second semiconductor layer of the first or third light emitting diode D**1** or D**3**, and a second pad **420** supplied with a negative power voltage V− is electrically connected to the upper electrode that is a cathode electrode of the sixth or eighth light emitting diode D**6** or D**8**.

According to the present invention described above, light generated in the active layer of each of the light emitting diodes is reflected from the lower and upper electrodes toward the substrate, and the flip-chip type light emitting diodes are electrically connected through wiring of the upper electrodes on a single substrate. Specifically, the upper electrode serves as wiring for achieving electrical connection between the first semiconductor layer of one of a pair of adjacent light emitting diodes and the second semiconductor layer of the other of the pair of adjacent light emitting diodes. In this case, the upper electrode includes a reflective conductive layer, thereby reflecting light emitted from a light-emitting layer to enhance light extraction efficiency.

The upper electrode is shielded from the outside through the second interlayer insulating layer. The first pad supplied with a positive power voltage is electrically connected to a lower electrode of a light emitting diode connected most closely to the positive power voltage. The second pad supplied with a negative power voltage is electrically connected to an upper electrode of a light emitting diode connected most closely to the negative power voltage.

Thus, it is possible to solve inconvenience in a process of mounting a plurality of flip-chip type light emitting diodes on a submount substrate and implementing two terminals to an external power source through wiring arranged on the submount substrate. In addition, the space between adjacent cell regions can be shielded by the upper electrode, thereby maximizing the reflection of light toward the substrate.

Further, the second interlayer insulating layer protects a laminated structure, which is arranged between the substrate and the second interlayer insulating layer, from external temperature or humidity and the like. Thus, it is possible to implement a structure that can be directly mounted on a substrate without intervention of any separate packaging means.

In particular, since a plurality of flip-chip type light emitting diodes are implemented on a single substrate, there is an advantage in that a commercial power source can be directly used while excluding a voltage drop, a conversion of voltage level or a conversion of waveform for the commercial power source.

Although the present invention has been described in connection with the preferred embodiments, the present invention is not limited thereto. Accordingly, it will be understood by those skilled in the art that various modifications and changes can be made thereto without departing from the spirit and scope of the invention defined by the appended claims.

The invention claimed is:

1. A light emitting diode array, comprising:

a growth substrate;

a plurality of light emitting diodes arranged on the substrate, each of the plurality of light emitting diodes having a first semiconductor layer, an active layer and a second semiconductor layer; and

a plurality of upper electrodes arranged on the plurality of light emitting diodes and formed of an identical material, each of the plurality of upper electrodes being electrically connected to the first semiconductor layer of a respective one of the light emitting diodes,

wherein at least one of the upper electrodes is electrically connected to the second semiconductor layer of an adjacent one of the light emitting diodes, and another of the upper electrodes is insulated from the second semiconductor layer of an adjacent one of the light emitting diodes,

wherein each of the light emitting diodes has a via hole for causing the first semiconductor layer to be exposed through the second semiconductor layer and the active layer, and

wherein each of the upper electrodes is connected to the first semiconductor layer of a respective one of the light emitting diodes through the via hole.

2. The light emitting diode array of claim **1**, wherein the upper electrodes comprise ohmic contact layers in ohmic contact with the first semiconductor layers.

3. The light emitting diode array of claim **2**, wherein the ohmic contact layers comprise any one metallic material selected from the group consisting of Cr, Ni, Ti, Rh and Al.

4. The light emitting diode array of claim **1**, wherein the ohmic contact layers comprise ITO.

5. The light emitting diode array of claim **2**, wherein the upper electrodes comprise reflective conductive layers positioned on the ohmic contact layers.

6. The light emitting diode array of claim **1**, further comprising a first interlayer insulating layers arranged between the light emitting diodes and the upper electrodes,

wherein the upper electrodes are insulated from side surfaces of the light emitting diodes by the first interlayer insulating layer.

7. The light emitting diode array of claim **6**, further comprising lower electrodes respectively arranged on the second semiconductor layers of the light emitting diodes,

wherein the first interlayer insulating layer exposes a portion of the lower electrode on each of the light emitting diodes, and

wherein the upper electrode(s) electrically connected to the second semiconductor layer of the adjacent light emitting diode is connected to the exposed portion of the lower electrode through the first interlayer insulating layer.

8. The light emitting diode array of claim **7**, wherein each of the lower electrodes comprises a reflective layer.

9. The light emitting diode array of claim **7**, further comprising a second interlayer insulating layer covering the upper electrodes,

wherein the second interlayer insulating layer exposes one of the lower electrodes and the upper electrode insulated from the second semiconductor layer of the adjacent light emitting diode.

10. The light emitting diode array of claim **9**, wherein the light emitting diodes are connected in series by the upper electrodes, and

wherein the second interlayer insulating layer exposes lower and upper electrodes corresponding to light emitting diodes at both ends of the light emitting diodes connected in series.

11. The light emitting diode array of claim **9**, further comprising first and second pads positioned on the second interlayer insulating layer, wherein the first pad is connected to the lower electrode exposed through the second interlayer insulating layer, and the second pad is connected to the upper electrode exposed through the second interlayer insulating layer.

12. The light emitting diode array of claim **1**, wherein the upper electrodes occupy at least 30% and less than 100% of the entire area of the light emitting diode array.

13. The light emitting diode array of claim **1**, wherein each of the upper electrodes is in the form of a plate or sheet having a ratio of length to width in a range of 1:3 to 3:1.

14. The light emitting diode array of claim **1**, wherein at least one of the upper electrodes has a length or width larger than that of a respective one of the light emitting diodes.

15. The light emitting diode array of claim **1**, wherein the upper electrodes comprise reflective conductive layers.

16. The light emitting diode array of claim **15**, further comprising a first interlayer insulating layers arranged between the light emitting diodes and the upper electrodes,

wherein the upper electrodes are insulated from side surfaces of the light emitting diodes by the first interlayer insulating layer.

17. The light emitting diode array of claim **16**, wherein the first interlayer insulating layer and the upper electrodes construct an omni-directional reflector.

18. The light emitting diode array of claim **16**, wherein the first interlayer insulating layer comprises a distributed Bragg reflector.

19. A method of forming a light emitting diode array, the method comprising:

forming a plurality of light emitting diodes, each of the plurality of light emitting diodes having a first semiconductor layer, an active layer and a second semiconductor layer on a growth substrate, wherein each of the plurality of light emitting diodes has the first semiconductor layer exposed by removing the second semiconductor layer and the active layer;

forming a first interlayer insulating layer for covering the light emitting diodes, wherein the first interlayer insulating layer exposes the exposed first semiconductor layers and has openings positioned on the second semiconductor layer of each of the light emitting diodes; and

forming a plurality of upper electrodes from an identical material on the first interlayer insulating layer,

wherein each of the upper electrodes is connected to the first semiconductor layer of a respective one of the light emitting diodes, and

wherein at least one of the upper electrodes is electrically connected to the second semiconductor layer of an adjacent one of the light emitting diodes through the opening of the first interlayer insulating layer, and another of the upper electrodes is insulated from the second semiconductor layer of an adjacent one of the light emitting diodes,

wherein each of the upper electrodes comprises a reflective conductive layer and the first interlayer insulating layer comprises a distributed Bragg reflector.

20. The method of claim **19**, further comprising:

forming lower electrodes on the second semiconductor layers of the respective light emitting diodes before the first interlayer insulating layer is formed.

21. The method of claim **20**, further comprising:

forming a second interlayer insulating layer on the upper electrodes,

wherein the second interlayer insulating layer exposes one of the lower electrodes and the other upper electrode insulated from the second semiconductor layer of the adjacent light emitting diode.

22. The method of claim **21**, further comprising:

forming first and second pads on the second interlayer insulating layer,

wherein the first pad is connected to the lower electrode, and the second pad is connected to the upper electrode.

23. The method of claim **19**, further comprising:

cutting the growth substrate into individual units,

wherein the upper electrodes occupy at least 30% and less than 100% of the area of the light emitting diode array of each of the cut individual units.

24. A light emitting diode array, comprising:

a growth substrate;

a plurality of light emitting diodes arranged on the substrate, each of the plurality of light emitting diodes having a first semiconductor layer, an active layer and a second semiconductor layer; and

a plurality of upper electrodes arranged on the plurality of light emitting diodes and formed of an identical material, each of the plurality of upper electrodes being electrically connected to the first semiconductor layer of a respective one of the light emitting diodes,

wherein at least one of the upper electrodes is electrically connected to the second semiconductor layer of an adjacent one of the light emitting diodes, and another of the upper electrodes is insulated from the second semiconductor layer of an adjacent one of the light emitting diodes,

wherein the light emitting diode array further comprises a first interlayer insulating layers arranged between the light emitting diodes and the upper electrodes, wherein the upper electrodes are insulated from side surfaces of the light emitting diodes by the first interlayer insulating layer,

wherein the light emitting diode array further comprises lower electrodes respectively arranged on the second semiconductor layers of the light emitting diodes, wherein the first interlayer insulating layer exposes a portion of the lower electrode on each of the light emitting diodes, and wherein the upper electrode(s) electrically connected to the second semiconductor layer of the adjacent light emitting diode is connected to the exposed portion of the lower electrode through the first interlayer insulating layer,

wherein the light emitting diode array further comprises a second interlayer insulating layer covering the upper electrodes, wherein the second interlayer insulating layer exposes one of the lower electrodes and the upper electrode insulated from the second semiconductor layer of the adjacent light emitting diode, and

wherein the light emitting diode array further comprises first and second pads positioned on the second interlayer insulating layer, wherein the first pad is connected to the lower electrode exposed through the second interlayer insulating layer, and the second pad is connected to the upper electrode exposed through the second interlayer insulating layer.

25. A light emitting diode array, comprising:

a growth substrate;

a plurality of light emitting diodes arranged on the substrate, each of the plurality of light emitting diodes having a first semiconductor layer, an active layer and a second semiconductor layer; and

a plurality of upper electrodes arranged on the plurality of light emitting diodes and formed of an identical material, each of the plurality of upper electrodes being electrically connected to the first semiconductor layer of a respective one of the light emitting diodes,

wherein at least one of the upper electrodes is electrically connected to the second semiconductor layer of an adjacent one of the light emitting diodes, and another of the upper electrodes is insulated from the second semiconductor layer of an adjacent one of the light emitting diodes,

wherein the upper electrodes comprise reflective conductive layers,

wherein the light emitting diode array further comprises a first interlayer insulating layers arranged between the light emitting diodes and the upper electrodes,

wherein the upper electrodes are insulated from side surfaces of the light emitting diodes by the first interlayer insulating layer, and

wherein the first interlayer insulating layer comprises a distributed Bragg reflector.

26. A method of forming a light emitting diode array, the method comprising:

forming a plurality of light emitting diodes, each of the plurality of light emitting diodes having a first semiconductor layer, an active layer and a second semiconductor layer on a growth substrate, wherein each of the plurality of light emitting diodes has the first semiconductor layer exposed by removing the second semiconductor layer and the active layer;

forming a first interlayer insulating layer for covering the light emitting diodes, wherein the first interlayer insulating layer exposes the exposed first semiconductor layers and has openings positioned on the second semiconductor layer of each of the light emitting diodes; and

forming a plurality of upper electrodes from an identical material on the first interlayer insulating layer,

wherein each of the upper electrodes is connected to the first semiconductor layer of a respective one of the light emitting diodes, and

wherein at least one of the upper electrodes is electrically connected to the second semiconductor layer of an adjacent one of the light emitting diodes through the opening of the first interlayer insulating layer, and another of the upper electrodes is insulated from the second semiconductor layer of an adjacent one of the light emitting diodes,

wherein the method further comprises forming lower electrodes on the second semiconductor layers of the respective light emitting diodes before the first interlayer insulating layer is formed,

wherein the method further comprises forming a second interlayer insulating layer on the upper electrodes, wherein the second interlayer insulating layer exposes one of the lower electrodes and the other upper electrode insulated from the second semiconductor layer of the adjacent light emitting diode, and

wherein the method further comprising forming first and second pads on the second interlayer insulating layer, wherein the first pad is connected to the lower electrode, and the second pad is connected to the upper electrode.

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